Claim Amendments

1. (Currently Amended) An apparatus, comprising:

an input-output interface to receive from an input-output device a first transaction associated with a first address;

an address queue coupled with said input-output interface to store a second address of a pending transaction;

address logic circuitry coupled with said address queue to compare the first address against the second address; and

ownership pre-fetch circuitry coupled with said address logic circuitry to initiate a request for an ownership of a first memory content associated with the first address for the first transaction unless the first address is substantially equivalent to the second address.

2. (Original) The apparatus of claim 1, further comprising a transaction queue coupled with said input-output interface to store a header for the pending transaction.

3. (Original) The apparatus of claim 1, further comprising a cache coupled with said input-output interface to store data of a memory line to anticipate a subsequent read transaction.

4. (Original) The apparatus of claim 3, further comprising read logic circuitry coupled with said input-output interface to attach cache line invalidation data to another read transaction to invalidate the read data.

5. (Original) The apparatus of claim 1, further comprising transaction bypass circuitry coupled with said input-output interface to allow the first transaction to advance upbound substantially independent of an advancement of the pending transaction, wherein the first address is different from the second address.

6. (Original) The apparatus of claim 5, wherein the transaction bypass circuitry comprises transaction bypass circuitry coupled with said input-output interface to the first transaction to advance upbound substantially independent of an advancement of the pending transaction, wherein a memory line address associated with the first transaction is different from a memory line address associated with the pending transaction.

7. (Original) The apparatus of claim 5, wherein the transaction bypass circuitry comprises transaction bypass circuitry coupled with said input-output interface to allow the first transaction to advance upbound substantially independent of an advancement of the pending transaction, wherein a first hub identification associated with the first transaction is different from a second hub identification associated with the pending transaction.

8. (Canceled).

9. (Original) The apparatus of claim 1, wherein said address queue comprises circuitry to associate the second address with the pending transaction.

10. (Original) The apparatus of claim 9, wherein the circuitry comprises memory to store an association with an entry in a transaction queue.

11. (Original) The apparatus of claim 1, wherein said address logic circuitry comprises circuitry to compare the first address against an invalidation address associated with the pending transaction to prevent the first transaction from bypassing the pending transaction, wherein the invalidation address is substantially equivalent to the first address.

12. (Original) The apparatus of claim 1, wherein said ownership pre-fetch circuitry comprises circuitry to initiate the request for the ownership before a transaction order of the first transaction is to satisfy an ordering rule.

13. (Currently Amended) A method, comprising:

receiving a first transaction from an input-output device via an ordered interface;

comparing a first address associated with the first transaction against a second address in an address queue, wherein the second address is associated with a second transaction; and

pre-fetching ownership of a memory content associated with the first address, wherein the first address is different from the second address.

14. (Original) The method of claim 13, further comprising comparing the first address to a cached address associated with a line of a cache, wherein the first transaction comprises a read transaction.

15. (Original) The method of claim 14, further comprising responding to the first transaction with the line of the cache, wherein the first address substantially matches the cached address.

16. (Original) The method of claim 14, further comprising attaching cache line invalidation data to the read transaction to invalidate the line of the cache.

17. (Original) The method of claim 13, further comprising advancing the first transaction to an unordered interface substantially independent of an advancement of the second transaction to the unordered interface, wherein the first address is different from the second address.

18. (Original) The method of claim 17, wherein advancing the first transaction comprises advancing a read transaction.

19. (Original) The method of claim 18, wherein advancing the first transaction comprises advancing a read transaction to the unordered interface substantially independent of the advancement of the second transaction unless a memory line address associated with the read transaction is substantially equivalent to a memory line address associated with the second transaction.

20. (Original) The method of claim 17, wherein advancing the first transaction comprises advancing the first transaction to the unordered interface substantially independent of the advancement of the second transaction, wherein a hub identification associated with the second transaction is different from a hub identification associated with the first transaction.

21. (Original) The method of claim 13, wherein said comparing a first address comprises comparing a first memory line address associated with the first transaction against a second memory line address associated with the second transaction.

22. (Original) The method of claim 13, wherein said comparing a first address comprises comparing a first hub identification of the first address against a second hub identification of the second address.

23. (Original) The method of claim 13, wherein said pre-fetching ownership comprises initiating a request for ownership of the memory content by the first transaction before the second transaction is to satisfy an ordering rule to transmit to the unordered interface.

24. (Currently Amended) A system, comprising:

an input-output interface to receive from an input-output device a first transaction associated with a first address;

an address queue coupled with said input-output interface to store a second address of a pending transaction;

address logic circuitry coupled with said address queue to compare the first address against the second address;

ownership pre-fetch circuitry coupled with said address logic circuitry to initiate a request for an ownership of a first memory content associated with the first address for the first transaction, wherein the first address is different from the second address;

a transaction queue coupled with said input-output interface to maintain a transaction order for the pending transaction; and

a memory device coupled with said transaction queue to respond to the pending transaction.

25. (Original) The system of claim 24, further comprising a scalability port switch coupled with said transaction queue to transmit the pending transaction to said memory device.

26. (Original) The system of claim 24, further comprising a bridge coupled with said input-output interface to couple more than one input-output device with said input-output interface.

27. (Currently Amended) A machine-readable medium containing instructions, which when executed by a machine, cause said machine to perform operations, comprising:

receiving a first transaction from an input-output device via an ordered interface;

comparing a first address associated with the first transaction against a second address in an address queue, wherein the second address is associated with a second transaction; and

pre-fetching ownership of a memory content associated with the first address, wherein the first address is different from the second address.

28. (Original) The machine-readable medium of claim 27, further comprising comparing the first address to a cached address associated with a line of a cache, wherein the first transaction comprises a read transaction.

29. (Original) The machine-readable medium of claim 27, wherein said comparing a first address comprises comparing a first hub identification of the first address against a second hub identification of the second address.

30. (Original) The machine-readable medium of claim 27, wherein said pre-fetching ownership comprises initiating a request for ownership of the memory content by the first transaction.